IN THE CLAIMS

1. (Currently Amended) A programmable delay cell comprising:

a capacitor coupled to a low supply rail;

a conductor coupled to an output of said programmable delay cell; and

two or more pass gates coupled in parallel to each other, wherein a first terminal of each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the capacitor. ~~to said conductor and to said capacitor.~~

2. (Original) The programmable delay cell of claim 1, wherein an impedance of each of said pass gates is to be controlled by a respective control signal.

3. (Original) The programmable delay cell of claim 1, further comprising:

a variable impedance transistor coupled to a high supply rail and to said conductor, wherein an impedance of said variable impedance transistor is to be determined by a control signal.

4. (Currently Amended) A programmable delay cell comprising:

a conductor coupled to an output of said programmable delay cell; [[and]]

a switch transistor coupled to the conductor; and

a variable impedance transistor coupled to a high supply rail and to ~~said conductor~~ a source terminal of the switch transistor, wherein an impedance of said variable impedance transistor is to be determined by a control signal.

5. (Original) The programmable delay cell of claim 4, wherein said control signal is set in response to output from a system to measure changes in the behavior of an integrated circuit

comprising said programmable delay cell, said changes resulting, at least in part, from variations in a supply voltage to said integrated circuit, variations in an ambient temperature and variations in a temperature of said integrated circuit.

6. (Original) The programmable delay cell of claim 4, wherein said control signal is a continuous signal.

7. (Currently Amended) A controller comprising:

an output buffer to generate an electrical signal on a conductor coupled to said controller; and

a programmable delay cell coupled to said output buffer, wherein said programmable delay cell includes at least:

a capacitor coupled to a low supply rail;

a conductor coupled to an output of said programmable delay cell; and

two or more pass gates coupled in parallel to each other, wherein a first terminal of each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the capacitor. ~~to said conductor and to said capacitor.~~

8. (Original) The controller of claim 7, further comprising:

a register coupled to said programmable delay cell to store a value that determines a time delay introduced by said programmable delay cell.

9. (Original) The controller of claim 8, further comprising:

a memory to store one or more values to program to said register.

10. (Original) The controller of claim 7, wherein said controller is a memory controller.

11. (Original) The controller of claim 7, further comprising:

one or two registers coupled to said output buffer to store a first value that determines the source driving impedance of said output buffer and to store a second value that determines the sink driving impedance of said output buffer.

12. (Currently Amended) A controller comprising:

an output buffer to generate an electrical signal on a conductor coupled to said controller; and

a programmable delay cell coupled to said output buffer, wherein said programmable delay cell includes at least:

a conductor coupled to an output of said programmable delay cell; [[and]]

a switch transistor coupled to the conductor; and

a variable impedance transistor coupled to a high supply rail and to a source terminal of the switch transistor ~~said conductor~~, wherein an impedance of said variable impedance transistor is to be determined by a control signal.

13. (Original) The controller of claim 12, wherein said control signal is set in response to output from a system to measure changes in the behavior of said controller, said changes resulting, at least in part, from variations in a supply voltage to said controller, variations in an ambient temperature and variations in a temperature of said controller.

14. (Original) The controller of claim 12, further comprising:

a register coupled to said programmable delay cell to store a value that determines a time delay introduced by said programmable delay cell.

15. (Original) The controller of claim 14, further comprising:

a memory to store one or more values to program to said register.

16. (Original) The controller of claim 12, wherein said controller is a memory controller.

17. (Original) The controller of claim 12, further comprising:

one or two registers coupled to said output buffer to store a first value that determines the source driving impedance of said output buffer and to store a second value that determines the sink driving impedance of said output buffer.

18. (Currently Amended) A controller comprising:

an input buffer to receive an electrical signal from a conductor coupled to said controller; and

a programmable delay cell coupled to said input buffer, wherein said programmable delay cell includes at least:

a capacitor coupled to a low supply rail;

a conductor coupled to an output of said programmable delay cell; and

two or more pass gates coupled in parallel to each other, wherein a first terminal of each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the capacitor. ~~to said conductor and to said capacitor.~~

19. (Original) The controller of claim 18, further comprising:

a register coupled to said programmable delay cell to store a value that determines a time delay introduced by said programmable delay cell.

20. (Original) The controller of claim 19, further comprising:

a memory to store one or more values to program to said register.

21. (Original) The controller of claim 18, wherein said controller is a memory controller.

22. (Currently Amended) A controller comprising:

an input buffer to receive an electrical signal from a conductor coupled to said controller; and

a programmable delay cell coupled to said input buffer, wherein said programmable delay cell includes at least:

a conductor coupled to an output of said programmable delay cell; [[and]]

a switch transistor coupled to the conductor; and

a variable impedance transistor coupled to a high supply rail and to a source terminal of the switch transistor ~~said conductor~~, wherein an impedance of said variable impedance transistor is to be determined by a control signal.

23. (Original) The controller of claim 22, wherein said control signal is set in response to output from a system to measure changes in the behavior of said controller, said changes resulting, at least in part, from variations in a supply voltage to said controller, variations in an ambient temperature and variations in a temperature of said controller.

24. (Original) The controller of claim 22, further comprising:

a register coupled to said programmable delay cell to store a value that determines a time delay introduced by said programmable delay cell.

25. (Original) The controller of claim 24, further comprising:

a memory to store one or more values to program to said register.

26. (Original) The controller of claim 22, wherein said controller is a memory controller.

27-33. (Withdrawn)

34. (Currently Amended) A printed circuit board comprising:

a graphics chip;

a controller including at least a programmable delay cell, said programmable delay cell including at least:

a capacitor coupled to a low supply rail;

a conductor coupled to an output of said programmable delay cell; and

two or more pass gates coupled in parallel to each other, wherein a first terminal of each of the two or more pass gates is coupled to the conductor and a second terminal of the each of the two or more pass gates is coupled to the capacitor. ~~to said conductor and to said capacitor.~~

35. (Original) The printed circuit board of claim 34, wherein an impedance of each of said pass gates is to be controlled by a respective control signal.

36. (Original) The printed circuit board of claim 34, wherein said programmable delay cell further includes:

a variable impedance transistor coupled to a high supply rail and to said conductor, wherein an impedance of said variable impedance transistor is to be determined by a control signal.

37-64. (Withdrawn)